IN THE CLAIMS

Please cancel claims 1 and 10 without prejudice or disclaimer, and amend claims 2, 4-7, 9 and 11-18 as follows:

1. (Cancelled)

2. (Currently Amended) [[The]] A semiconductor integrated circuit device ~~according to claim 1~~ comprising;

a first circuit block having first and second modes;

a second circuit block; and

an interface circuit provided between an output of the first circuit block and an input of the second circuit block;

wherein the interface circuit includes a storage unit to hold a state of the output of the first circuit block and a signal gate unit which is provided between the storage unit and the output of the first circuit block,

wherein a first supply voltage is applied to the first circuit block in the first mode and the first supply voltage is stopped to apply to the first circuit block in the second mode,

wherein the signal gate unit connects the storage unit to the output of the first circuit block in the first mode and the signal gate unit disconnects the storage unit from the output of the first circuit block in the second mode,

wherein the first circuit block includes a plurality of registers, and

wherein values of the registers are saved when the first circuit block changes from the first mode to the second mode.

3. (Original) The semiconductor integrated circuit device according to claim 2, further comprising: a memory to save the values of the registers.

4. (Currently Amended) The semiconductor integrated circuit device according to claim 2, wherein the interface circuit further includes a comparator ~~("CMP")~~ to compare the state of the output of the first circuit block and a state of the input of the second circuit block,

wherein, when the first circuit block changes from the second mode to the first mode, the values of the registers are restored to the registers of the first circuit block ~~(S8 in Fig. 2)~~ and the state of the output of the first circuit block becomes stable based on the restored values of the registers, and

wherein, when the state of the output of the first circuit block based on the restored values of the registers matches the state of the input of the second circuit block, the signal gate unit is controlled to connect the storage unit to the output of the first circuit block.

5. (Currently Amended) The semiconductor integrated circuit device according to claim [[1]]2, further comprising:

a first area ~~("main power source area")~~; and

a second area ~~("sub-power source area")~~ electrically separated from the first area[[;]],

wherein the first circuit block is provided in the first area and the interface circuit ~~block~~ is provided in the second area.

6. (Currently Amended) The semiconductor integrated circuit device according to claim 5, further comprising:

a third area ~~("power source line area")~~; and

~~wherein~~ a power supply line to supply the first supply voltage to the first circuit block, ~~is provided in the power supply line and~~

wherein the third area is provided to surround the first area and the second area is provided to surround the third area[[,]].

7. (Currently Amended) The semiconductor integrated circuit device according to claim [[1]] 2, wherein a second power supply voltage is applied to the interface circuit and a third power supply voltage is applied to the second circuit block.

8. (Original) The semiconductor integrated circuit device according to claim 7, wherein the first, second and third power supply voltages are controlled by an external power device.

9. (Currently Amended) The semiconductor integrated circuit device according to claim 7, wherein the second power supply voltage is equal to the first power supply voltage and the third power supply voltage is higher than the first power supply voltage, and

wherein the second circuit block includes an I/O circuit.

10. (Cancelled)

11. (Currently Amended) [[The]] A semiconductor integrated circuit device ~~according to claim 10~~ comprising:

a first circuit block;

a second circuit block; and

an interface circuit provided between an output of the first circuit block and an input of the second circuit block;

wherein the interface circuit includes a storage unit to hold a state of the output of the first circuit block and a signal gate unit which is provided between the storage unit and the output of the first circuit block,

wherein the signal gate unit connects the storage unit to the output of the first circuit block when a first power supply is applied to the first circuit block and the signal gate unit disconnects the storage unit from the output of the first circuit block when the first power supply is stopped to apply to the first circuit block,

wherein the first circuit block includes a plurality of registers, and

wherein values of the registers are saved before the first power supply is stopped to apply the first circuit block.[[.]]

12. (Currently Amended) The semiconductor integrated circuit device according to claim 11, further comprising[[;]]: a memory to save the values of the registers.

13. (Currently Amended) The semiconductor integrated circuit device according to claim 11, wherein the interface circuit further includes a comparator to compare the state of the output of the first circuit block and a state of the input of the second circuit block,

wherein, when the power supply voltage is applied to the first circuit block again, the values of the registers are restored to the registers of the first circuit block and the state of the output [[or]] of the first circuit block becomes stable based on the restored values of the registers, and

wherein, when the state of the output of the first circuit block based on the restored values of the registers matches the state of the input of the second circuit block, the signal gate unit is controlled to connect the storage unit to the output of the first circuit block ~~Mock~~.

14. (Currently Amended) The semiconductor integrated circuit device according to claim [[10]]11, further comprising:

a first area; and

a second area electrically separated from the first area;

wherein the first circuit block is provided in the first area and the interface circuit ~~block~~ is provided in the second area.

15. (Currently Amended) The semiconductor integrated circuit device according to claim 14, further comprising:

a third area; and

~~wherein~~ a power supply line to supply the first supply voltage to the first circuit block, ~~is provided in the power supply line and~~

wherein the third area is provided to surround the first area and the second area is provided to surround the third area.

16. (Currently Amended) The semiconductor integrated circuit device according to claim [[10]] 11, wherein a second power supply voltage is applied to the interface circuit and a third power supply voltage is applied to the second circuit block.

17. (Currently Amended) The semiconductor integrated circuit device according to claim 16, wherein the first, second and third power supply voltages are controlled by an external power device[[,]].

18. (Currently Amended) The semiconductor integrated circuit device according to claim 16, wherein the second power supply voltage is equal to the first power supply voltage and the third power supply voltage is higher than the first power supply voltage, and

wherein the second circuit block includes an I/0 Circuit.